

WHAT IS CLAIMED IS:

1. A static random access memory (SRAM) control circuit with a power saving function, which uses a chip select signal, an output enable signal and a write enable signal to control memory read and write, wherein
5 the SRAM control circuit performs a read operation when the chip select signal and the output enable signal are active and performs a write operation when the chip select signal and the write enable signal are active, the SRAM control circuit comprising:

a memory unit for storing data;
10 an address decoder for decoding address on address lines and accordingly outputting an address signal to select a specific memory area in the memory unit;

a buffer for buffering data to be accessed such that, when performing a read operation, data in the specific memory area is buffered in
15 the buffer to output, and when performing a write operation, inputted data is buffered in the buffer for being written to the specific memory area;

an address register for storing a current address signal generated by the address decoder and outputting a previous address signal;

an address comparator for comparing the current address signal and
20 the previous address signal; and

a mark logic for masking the chip select signal when the current address signal is the same as the previous address signal, wherein the buffer directly outputs buffered data.

2. The SRAM control circuit as claimed in claim 1, wherein the chip

select signal, the output enable signal and the write enable signal are active at a low level and inactive at a high level.

3. The SRAM control circuit as claimed in claim 2, wherein the address comparator outputs a signal with a low level when the current
5 address signal and the previous address signal are the same and otherwise the address comparator outputs a signal with a high level.

4. The SRAM control circuit as claimed in claim 3, wherein the mask logic is constituted by a NOR gate and an OR gate, the NOR gate receiving an output of the address comparator and the output enable signal,
10 the OR gate applying an OR operation to an output of the NOR gate and the chip select signal.